IN THE CLAIMS:

Please cancel claims 1-24 after adding new claims 25-41 herein. Please note that all claims currently pending and under consideration in the referenced application are shown below. Please enter these claims as amended. This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

Claims 1-24. (canceled)

25. (new) A method of generating delay locked clocks, comprising:

determining a first phase difference between a clock signal and a first delayed clock signal to ascertain a first delay magnitude;

delaying the clock signal by the first delay magnitude to generate the first delayed clock signal substantially synchronized to the clock signal;

determining a second phase difference between an inverse clock signal and a second delayed clock signal to establish a second delay magnitude;

delaying the first delayed clock signal by the second delay magnitude to generate the second delayed clock signal substantially synchronized to the inverse clock signal.

26. (new) The method of claim 25, further comprising generating a timing signal by generating a rising edge of the timing signal in response to the first delayed clock signal and generating a falling edge of the timing signal in response to the second delayed clock signal.

27. (new) The method of claim 26, wherein the rising edge of the timing signal is generated in response to a rising edge of the first delayed clock signal.

28. (new) The method of claim 26, wherein the falling edge of the timing signal is generated in response to a rising edge of the second delayed clock signal.

29. (new) The method of claim 26, wherein determining the first phase difference comprises comparing a rising edge of the clock signal with a rising edge of the timing signal generated in response to the first delayed clock signal.

30. (new) The method of claim 29, further comprising asserting a phase-lock signal when the first phase difference is substantially near zero.

31. (new) The method of claim 30, wherein determining the second phase difference is initiated in response to the assertion of the phase-lock signal.

32. (new) The method of claim 26, wherein determining the second phase difference comprises comparing a rising edge of the inverse clock signal with a falling edge of the timing signal generated in response to the second delayed clock signal.

33. (new) A method, comprising:

generating a first delayed clock signal by delaying a clock signal in response to at least one first control signal;

generating a pair of second delayed clock signals by delaying the first delayed clock signal in response to at least one second control signal;

generating a timing signal in response to the pair of second delayed clock signals;

generating the at least one first control signal by phase comparing the clock signal and the timing signal; and

generating the at least one second control signal by phase comparing an inverse clock signal and an inverted version of the timing signal.

34. (new) The method of claim 33, wherein generating the pair of second delayed clock signals comprises:

generating a first of the pair of second delayed clock signals by delaying the first delayed clock signal by a predetermined amount; and

generating a second of the pair of second delayed clock signals by delaying the first delayed clock signal by a variable amount in response to the at least one second control signal.

35. (new) The method of claim 34, wherein generating the timing signal comprises:

generating a rising edge of the timing signal in response to the first of the pair of second delayed clock signals; and

generating a falling edge of the timing signal in response to the second of the pair of second delayed clock signals.

36. (new) A synchronizing circuit, comprising:

a first phase detector configured to generate at least one first control signal related to a first phase comparison of a clock signal and a first delayed clock signal;

a first delay line configured to generate the first delayed clock signal as a delayed version of the clock signal by a first delay magnitude related to the at least one first control signal;

a second phase detector configured to generate at least one second control signal related to a second phase comparison of an inverse clock signal and a second delayed clock signal; and

a second delay line configured to generate the second delayed clock signal as a delayed version of the first delayed clock signal.

37. (new) The synchronizing circuit of claim 36, further comprising circuitry coupled to the first delay line and the second delay line, the circuitry configured to create a first edge of a timing signal in response to the first delayed clock signal and a second edge of the timing signal in response to the second delayed clock signal.

38. (new) The synchronizing circuit of claim 37, wherein the circuitry coupled to the first delay line is coupled through a third delay line.

39. (new) The synchronizing circuit of claim 38, wherein the third delay line is configured to add a third delay magnitude of a predetermined amount to the first delay magnitude of the first delayed clock signal.

40. (new) An electronic system comprising:

a processor;

a memory device associated with the processor; and

at least one of an input device, an output device and a data storage device associated with the processor;

wherein at least one component of the electronic system comprises a synchronizing circuit comprising:

a first phase detector configured to generate at least one first control signal related to a first phase comparison of a clock signal and a first delayed clock signal;

a first delay line configured to generate the first delayed clock signal as a delayed version of the clock signal by a first delay magnitude related to the at least one first control signal;

a second phase detector configured to generate at least one second control signal related to a second phase comparison of an inverse clock signal and a second delayed clock signal; and

a second delay line configured to generate the second delayed clock signal as a delayed version of the first delayed clock signal.

41. (new) A semiconductor substrate comprising structures configured to synchronize data to a system clock signal, the structures comprising:

a first phase detector configured to generate at least one first control signal related to a first phase comparison of a clock signal and a first delayed clock signal;

a first delay line configured to generate the first delayed clock signal as a delayed version of the clock signal by a first delay magnitude related to the at least one first control signal;

a second phase detector configured to generate at least one second control signal related to a second phase comparison of an inverse clock signal and a second delayed clock signal; and

a second delay line configured to generate the second delayed clock signal as a delayed version of the first delayed clock signal.